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Implementation of High Performance Comparator in 90nm Technology

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Abstract

In this paper a CMOS Differential current sensing comparator along with the Buffer stage has been introduced. In this paper comparator is implemented in a standard TSMC 90nm CMOS technology using Mentor Graphics Tool The simulation is carried out in 90nm technology. The supply voltage for this comparator is ± 0.9v.

This paper firstly elaborate about basic introduction of Comparator. Next section elaborate Different Current Sensing Comparator and Buffer Stage. Next section elaborate the design of comparator . Last section consist simulation results.

Keywords: Buffer stage, current sensing comparator, latch comparator.

Introduction

A Comparator is a circuit which compares the two analog signal and gives the output in the digital form, either logic '1' or logic '0' depending on the comparison. Comparators are most probably second most widely used electronic components after operational amplifiers in this world. Comparators are known as 1-bit analog-to digital converter and for that reason they are mostly used in large abundance in A/D converter. In the past, pre-amplifier based comparators have been used for ADC architectures such as flash and pipeline. The main drawback of pre-amplifier based comparators is the more offset voltage. To overcome this problem, dynamic comparators are often used that make a comparison once every clock period and require much less offset voltage. Due to low-offset, fast speed, low power consumption ,high input impedance, CMOS dynamic latched comparator are very attractive for many applications such as high speed analog-to-digital convertors(ADCs), memory sense amplifiers(SAs) and data receivers.

Differential Current Sensing Comparator

Fig.l shows the circuit diagram of the differential current sensing comparator. The circuit enters in regenerative mode whenever the Clk signal goes low. Transistor M12 is on and M7 is off. When values of both the outputs Out+ and Outincreasesabove threshold voltage of nMOS M5 and M6, both will start conducting which will connect the outputs with comparing circuit at the input side. It consumes more power because unless and until final state is reached both the outputs have to drive common mode currents.

The comparing circuit used at the input side consisting of transistors Ml, M2, M3 and M4 are used to transfer the difference of the input voltage into differential currents. During reset interval, a pass transistor M7 is used to connect both the outputs together.

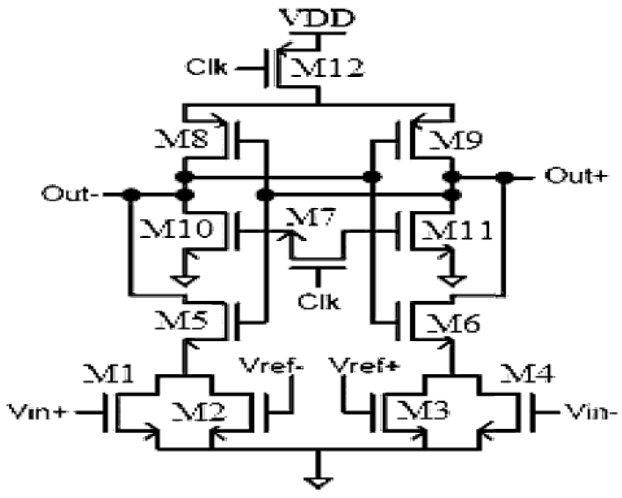

Fig.1.Differential current sensing comparator[1]

Buffer Stage

The schematic of output buffer circuit used in the comparator is shown in figure 2[5]. The output buffer stage is also known as post amplifier. This circuit is self biasing differential amplifier which has

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differential inputs as Vout+ & Vout- and does not have any slew rate
limitations. It is also useful in giving the output in proper shape.

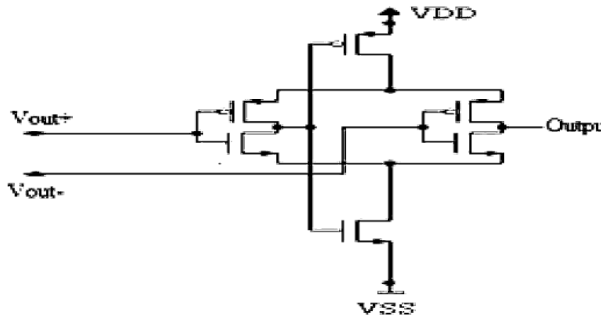

Fig.2 The Output Buffer Circuit[1]

Designing of the Comparator

The circuit diagram of Differential current sensing comparator along with the buffer stage is as shown in fig.2. The two outputs Out+ and Out- of differential current sensing comparator are being converted into single output with the output buffer circuit so that various analysis can be carried out. Table I given below shows different widths of the transistor to be used according to the chosen technology. The length for the transistor is 0.lum for 90nm technology.

Table 1.
cmos transistor widths for 90nm technologies

Technology	Wp(um)	Wn(um)
90nm	0.12	0.12

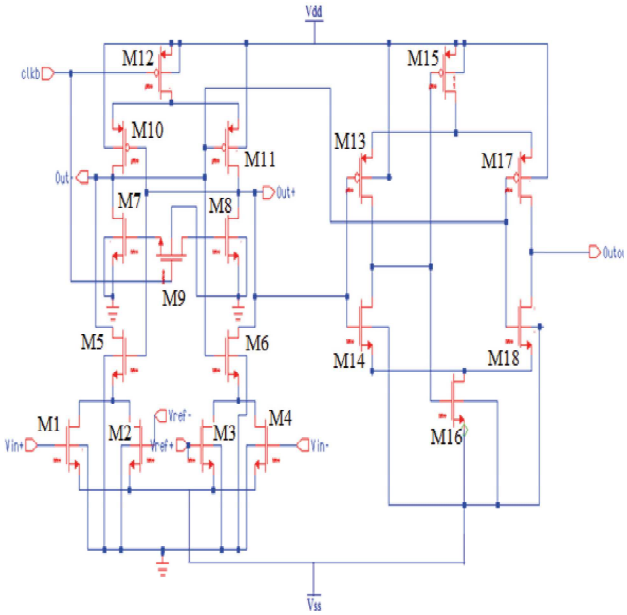

Fig.4 Design of Comparator

Different Characteristics of the Comparator

A. Propagation Delay for the comparator

The propagation delay is the time required for the change in output with respect to the change in input. The speed of the comparator is decided by the propagation delay of the comparator. Speed and propagation delay are inversely proportional to each other. If the propagation delay is higher, speed of the comparator will be slower and vice-versa. The propagation delay has been found in fig.5 and fig.10 from the transient response of the comparator for two different technologies.

B. Input common mode range(ICMR) for the comparator

ICMR- Input common mode range is the range of the input common mode voltage for which the comparator functions properly. This input common mode range is the range where all the transistors of the comparator are in saturation. Fig.8 shows simulated waveforms for ICMR for both of the technologies.

C. Offset voltage of the comparator

The output changes as the input difference crosses zero. If the output did not change until the input difference reached a value +Vos[4], then this difference would be defined as the offset voltage.Effect of offset can be reduced but cannot be avoided totally. The simulated waveforms for two different technologies measuring the offset voltage is as shown in fig.7.

Simulation Results

Table ii
voltage values for 90nm technology

Votage Terminals	Technology
VDD	1v
VSS	-1v
Vin+	0.9v.
Vin-	-0.9v
Vref+	0.45v
Vref-	-0.45v
clkb	-0.9v

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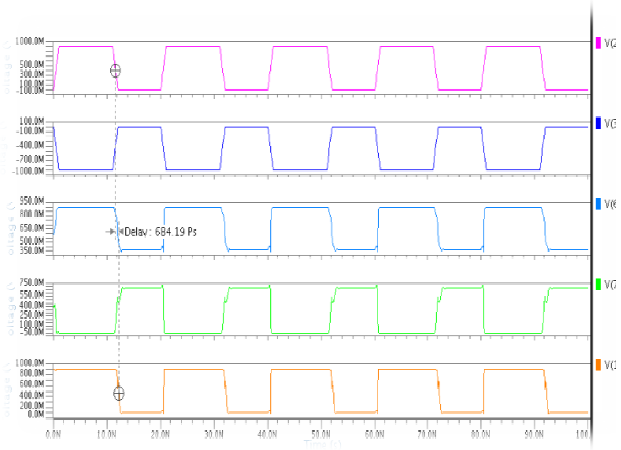

Fig. 5 Transient response.

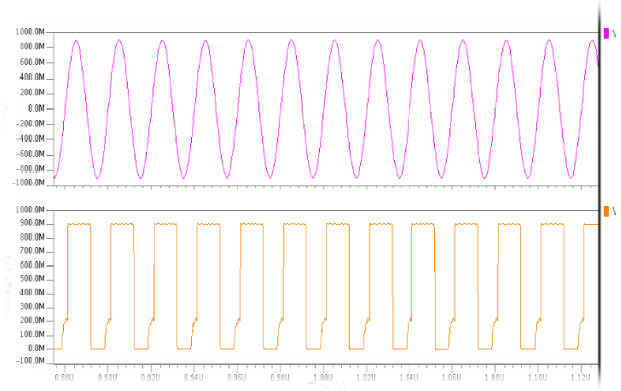

Fig. 6 Input as sine wave

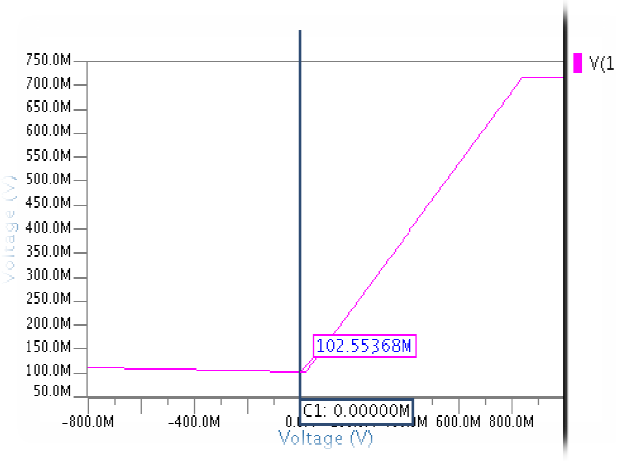

Fig.7 Offset

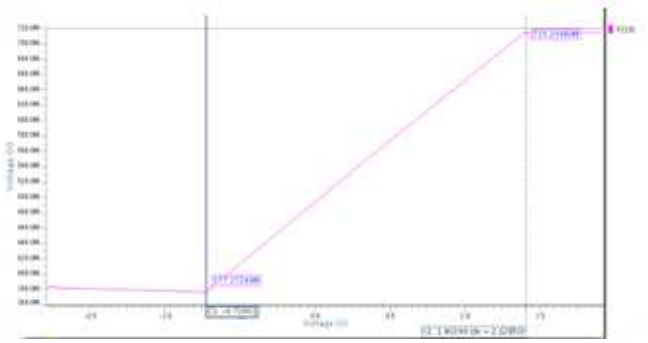

Fig.8 ICMR

Table III
Simulated Results

Parameters	Result
Propagation Delay(ns)	0.68
Power Dissipation(mW)	6.12
ICMR(V)	-0.7 to 1.4
Offset(mV)	0.10

Conclusion

In present work, high performance comparator is designed and simulated in 90nm CMOS Technology. The circuits are simulated in SPICE with MOSIS Level-60 MOS model parameters. After simulation Propagation Delay is 0.68ns, Power Dissipation is 6.12mW, ICMR is between -0.7V to 1.4V, and offset value is 0.10mV.

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